REMARKS

Claims 1-9 and 11 are pending; claim 10 has been canceled; claim 5 has been amended in several particulars; and claim 11 is newly added in accordance with current Office policy, to alternatively define Applicant's invention and thereby assist the Examiner by facilitating the search and thus expediting the compacted prosecution.

The Examiner states, "It appears that at least one full name of applicant Byoung-Han Kim is not present either in the signature or elsewhere in the papers." Note, however, that the Declaration filed 18 June 1997 and refiled on 29 September 1997 does include the full name of the inventor Byoung-Han Kim. A copy of the Declaration highlighting the inventors full name and the post card receipt is attached hereto. We respectfully ask that the PTO not loose this copy as it apparently has lost all the other copies.

In paragraph 2 on page 2 of Paper No. 5 and Paper No. 9, the Examiner has indicated that the Applicant is required to submit a proposed drawing correction in reply to the Office action. Note that the Examiner has not made any objections to the drawings which require such a proposed drawing correction, which are to be made in red. The Examiner then indicates that formal correction of the noted defect can be deferred and refers the Applicant to PTO FORM 948. Note that form 948 indicates that the left margin in Figs. 5, 6 and 17 are not acceptable. This cannot be corrected in a "proposed drawing correction" because such a proposed drawing correction is required to be shown in RED. The Examiner is respectfully requested to inform the Applicant how a proposed drawing correction in red can be provided for correcting the margins, or since the defects noted on PTO

FORM 948 are matters directed to form, *i.e.*, requiring formal correction, then the Applicant respectfully requests that requirement for correction be deferred until the application is allowed at which time new formal drawings correcting for the defects identified in Form 948 will be filed.

Claims 5 and 10 were rejected under 35 U.S.C. §112, second paragraph based upon a number of deficiencies kindly noted by the Examiner. Accordingly the above amendment is believed to correct for those deficiencies.

Claim 5 was rejected under 35 U.S.C. §102(e) as being anticipated by Koh. The applicant respectfully traverses this rejection for the following reason(s).

Claim 5 calls for *means for detecting a first resolution signal indicative of a resolution of said first display signal using horizontal and vertical synchronization signals related to said first display*. The Examiner has referred to Fig. 11(36), the selector of memory controller (2a), col. 9, lines39-64 and col. 10, lines 34-50, in Koh.

Koh discloses, "Explanation will first be given regarding the S/P converters 10a. One S/P converter 10a is provided for each of the three colors, red, green and blue. Each S/P converter 10a has a shift register 34 of 8-bit width and a latch circuit 35 of 8-bit width. A difference with the S/P converter 10 shown in FIG. 8a is that the output is not split between even bits and odd bits. One memory controller 2a is provided for each bit of each output data line (of 8-bit width) of the S/P converter 10a, for a total of eight. An 8-to-1 selector 36 is provided in each memory controller 2a. Gray-scale data (of 8-bit width) from the gray-scale pattern generator is inputted to the data input

terminal of this selector 36. In addition, based on the signals inputted from these three data lines, each data line being outputted from each S/P converter 10a, the selector 36 carries out the selection operation. The output (of 1-bit width) from each memory controller 2a is connected to the frame buffer memory 38 by means of a respective bi-directional buffer 37. The frame buffer memory 38 is a 256 Kbit (32 Kbyte) memory. The area within the frame buffer memory 38 from the 0000 address to the 3E7F address is used for storing the gray-scale pattern data corresponding to the CRT display data for the lower half of the screen, and the area from address 4000 to address 7E7F is used to store the gray-scale pattern data corresponding to the upper half of the screen."

Koh further discloses, "The selector 36 of the memory controller 2a selects the gray-scale data (of 8-bit width) based on the display data for CRT use. The selected gray-scale pattern data is written to the 4000 address of the frame buffer memory 38 in accordance with the write enable signal WE0. This address corresponds to the upper half of the screen. At this time, the gray-scale pattern data displayed in the upper half of the LCD panel 72 and the gray-scale pattern data displayed in the lower half of the LCD panel 72 are complete. Four dots are displayed on both the upper half and lower half of the LCD panel 72 at the same timing. At this point, selection is made of the upper four bits or the lower four bits of the eight bits according to selectors 42 and 43 within the LCD controller 3a. The gray-scale pattern, made 4 bits wide, is synchronized with shift clock CL2 and outputted to the LCD panel 72 by means of registers 44 and 45."

There is no disclosure in Koh, as can be seen from the above passages relied on in the rejection, of *means for detecting a first resolution signal indicative of a resolution of said first display signal using horizontal and vertical synchronization signals related to said first display signal.* In the passages of Koh relied on by the Examiner, there is no mention of the word *resolution*,

and there is no mention of *horizontal and vertical synchronization signals*. Note that in order for an anticipation rejection to be proper, the anticipating reference must disclose exactly what is claimed. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Note here that the Examiner has not relied on "inherency," accordingly, each and every element must be expressly described in Koh.

Claim 5 also calls for *means for comparing said first resolution signal with a second resolution signal indicative of a reference resolution.* Here, the Examiner states, "Koh discloses . . .means for comparing first resolution signal by the frame buffer memory (column 9; lines 58-67, and column 10; lines 1-17)."

First, it is not understood how a frame buffer memory can perform a comparison step. Second, Koh discloses, "The area within the frame buffer memory 38 from the 0000 address to the 3E7F address is used for storing the gray-scale pattern data corresponding to the CRT display data for the lower half of the screen, and the area from address 4000 to address 7E7F is used to store the gray-scale pattern data corresponding to the upper half of the screen. Data signals of 8-bit width from the frame buffer memory 38 are inputted to the LCD controller 3a by way of respective bi-directional buffers 37. The LCD controller 3a comprises three registers of 8-bit width 39, 40 and 41, two registers of 4-bit width 44 and 45, and two selectors 42 and 43. Registers 39_ 41 are latch circuits synchronous with signal PLAT1, and registers 44 and 45 are latch circuits synchronous with

shift clock signal CL2. 8-bit parallel data from the frame buffer memory 38 is inputted to the two registers 39 and 40. Register 41 is provided on the output side of register 39. The out puts of registers 40 and 41 are connected to registers 44 and 45 by means of selectors 42 and 43, respectively. Each of the selectors 42 and 43 are equipped with four 2-to-1 selector elements, and as will be explained hereinafter, are used to simultaneously display the data for the upper half of the screen and the data for the lower half of the screen. The outputs of registers 44 and 45 are outputted to the LCD panel 72 as upper screen display data UD0 to UD3 and lower screen display data LD0 to LD3."

The foregoing excerpt of Koh, relied on by the Examiner for anticipation, fails to disclose that the frame buffer memory performs a comparison of a first resolution signal with a second resolution signal, as erroneously asserted by the Examiner. In fact, there is no disclosure of any element in Koh that has a function of performing a comparison. Accordingly, Koh fails to disclose *means for comparing said first resolution signal with a second resolution signal indicative of a reference resolution.*

Claim 5 also calls for *means for converting said first display signal of serail format into said second display signal of parallel format, if there is a difference between said first and said second resolution signals.* Here, the Examiner states, "Koh discloses . . .means for converting first resolution signal (Figure 1(59), column 1; lines 54-56), and S/P circuit (Figure 2(10), column 5; lines 39-48)."

Actually, Koh discloses:

- " an S/P converter circuit 59 for converting the serial data of each color signal

to parallel data"; and

- "Each S/P converter 10 takes in the display video signal in serial format originally intended for output to the CRT and converts this display data to parallel format. Each S/P converter 10 receives an input of signal PLAT1 for control and red, green or blue display data. Parallel data (of 8-bit width) is outputted from the S/P converters 10, and in order to choose either gray-scale pattern A or gray-scale pattern B, this parallel data is split between each even-bit and odd-bit signal line EVEN, ODD. Each signal line EVEN, ODD is of 4-bit width."

As can be seen from the foregoing excerpts of Koh, relied on by the Examiner in the rejection, there is no "condition" placed on the serial-to-parallel converters for controlling when the converters convert a serial signal to a parallel signal. In claim 5 the "condition" is *if there is a difference between said first and said second resolution signals* then the first display signal of serail format is converted into a second display signal of parallel format. Tthe Examiner fails to show where such a "condition" is disclosed in Koh. Note, *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

Accordingly, Koh fails to disclose *means for converting said first display signal of serail format into said second display signal of parallel format, if there is a difference between said first and said second resolution signals.*

Therefore, the rejection of claim 5 is deemed to be in error and should be withdrawn.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

Respectfully submitted,

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